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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,746	07/16/2003	Weiguang Qiu	AME-007	1811

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EXAMINER

TRAN, THUY V

ART UNIT	PAPER NUMBER
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2821

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/621,746

Applicant(s)

QIU, WEIGUANG

Examiner

Thuy V. Tran

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on amendment filed 07/19/2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This is a response to the Applicant's amendment filed on July 19th, 2004. In virtue of this amendment, claims 1-9 are currently presented in the instant application.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Gray (Pub. No.: US 2003/0160574 A1).

With respect to claim 1, Gray discloses, in Fig. 2A, a system and a method for optimizing performance of a cold cathode fluorescent lamp (CCFL) circuit [270], wherein the CCFL circuit includes a CCFL [110] and a piezoelectric transformer [108] for driving the CCFL [110]; the method comprises providing (via output driver [201]) a driving waveform to the CCFL circuit [270] (see paragraph [0046], lines 3-4), wherein (i) a frequency of the driving waveform is based on a linearly translated input source voltage (which is provided by [101]; see paragraph [0046], lines 19-23 and paragraph [0060], lines 1-2), and (ii) a duty cycle of the driving waveform (performed by feedback loop [118] and circuit [233]) is based on a detected current through the

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CCFL (which is proportional to the voltage across resistor [113]; see paragraph [0049], lines 1-3).

With respect to claim 2, Gray discloses that the linearly translated input source voltage (which is provided by [101]) is based on characteristics of the PZT in the CCFL circuit (see Fig. 2A).

With respect to claim 3, Gray discloses that the linearly translated input source voltage (which is provided by [101]) is based on a potential input voltage range (which is VR1 ranging from 0.5 to 3 Volts; see paragraph [0050], lines 5-6) for the CCFL circuit [270].

With respect to claim 4, Gray discloses that providing the driving waveform includes turning on/off transistors of a half-bridge [104, 105] in the CCFL circuit.

With respect to claim 5, Gray discloses, in Fig. 2A, a system and a method for optimizing performance of a cold cathode fluorescent lamp (CCFL) circuit [270], wherein the CCFL circuit includes a CCFL [110] and a piezoelectric transformer [108] for driving the CCFL [110]; the method comprises (1) before operation of the CCFL circuit, determining a frequency of a driving waveform to the CCFL circuit [270] (based on the second control loop including [230, 216, 217], see paragraph [0046], lines 10-17; or the input source voltage provided by [101], see Fig. 2A), wherein (i) the frequency is based on a range of input source voltages (which is VR1 ranging from 0.5 to 3 Volts; see paragraph [0050], lines 5-6) and a range of desired linearly translated source voltages associated with the PZT (which is provided by battery source [101]; see paragraph [0060], lines 1-9), and (2), during operation of the CCFL circuit, adjusting a duty cycle of the driving waveform based on a detected current through the CCFL (which is proportional to the voltage across resistor [113]; see paragraph [0049], lines 1-3).

With respect to claim 6, Gray discloses, in Fig. 2A, a system for optimizing performance of a cold cathode fluorescent lamp (CCFL) circuit [270], wherein the CCFL circuit includes a CCFL [110] and a piezoelectric transformer [108] for driving the CCFL [110]; the system comprises (1) means [230, 216, 217, 220, 223, 224, 101] for determining a frequency of a driving waveform for the CCFL circuit [270], wherein the frequency is based on a range of input source voltages (which is VR1 ranging from 0.5 to 3 Volts; see paragraph [0050], lines 5-6) and a range of desired linearly translated source voltages associated with the PZT [108] (which is provided by battery source [101]; see paragraph [0060], lines 1-9), and (2) means [118, 233] for adjusting a duty cycle of the driving waveform based on a detected current through the CCFL (which is proportional to the voltage across resistor [113]; see paragraph [0049], lines 2-3).

With respect to claim 7, Gray discloses, in Fig. 2A, that the means for determining the frequency of the driving waveform includes (1) a first resistor [216] coupled between a node [N6] and a high voltage source (which is VOH, high level of signal OUTAPB; see paragraph [0056], lines 2-3), wherein the high voltage source is one voltage in the range of input source voltages, (2) a second resistor [217] coupled between the node and a low voltage source, (3) an error amplifier [213] having a positive input terminal connected to a reference voltage [VR2] and a negative input terminal, and (4) a third resistor [215] coupled to the node, the negative input terminal of the error amplifier, and an output terminal of the error amplifier.

With respect to claim 8, Gray discloses, in Fig. 2A, a linear voltage translator comprising (1) a first resistor [216] coupled between a node [N6] and a high voltage source (which is VOH, high level of signal OUTAPB; see paragraph [0056], lines 2-3), wherein the high voltage source is one voltage in the range of input source voltages, (2) a second resistor [217] coupled between

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the node [N6] and a low voltage source, (3) an error amplifier [230] having a positive input terminal connected to a reference voltage [VR2] and a negative input terminal, and (4) a third resistor [215] coupled to the node, the negative input terminal of the error amplifier, and an output terminal of the error amplifier.

With respect to claim 9, Gray discloses, in Fig. 2A, that the output terminal of the error amplifier [213] provides a signal [VCO_CONTROL] to a voltage controlled oscillator (VCO) [220] to determine an output frequency of the VCO.

Citation of relevant prior art

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Kernahan et al. (Pub. No.: US 2004/0095117 A1) discloses a control circuit and method for driving a CCFL.

Prior art Terada et al. (Pub. No.: US 2004/0021492 A1) discloses a pulsed width modulation circuit.

Prior art Kohn (U.S. Patent No. 6,747,421) discloses self-oscillation circuits.

Prior art Vasquez Carazo et al. (U.S. Patent No. 6,617,757) discloses a circuit including a piezoelectric transformer.

Prior art Wells et al. (U.S. Patent No. 6,400,096) discloses a control circuit for a piezoelectric transformer for a fluorescent lamp.

Prior art Boyd (U.S. Patent No. 6,278,625) discloses an inverter circuit with multilayer piezoelectric transformer.

Prior art Honbo et al. (U.S. Patent No. 5,886,477) discloses a driver for CCFL.

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Prior art Williams (U.S. Patent No. 5,548,189) discloses a power supply and a control circuit for driving a fluorescent lamp.

Prior art Harford (U.S. Patent No. 3,579,133) discloses a signal translating stage.

Remarks and conclusion

4. Applicant's arguments filed on July 19th, 2004 have been fully considered but they are not persuasive.

With respect to Applicant's arguments on amended claim 1 in the second, third, fourth, and fifth paragraphs at page 5 of the amendment, the Examiner respectfully disagrees with Applicant's statement, which is "Gary fails to disclose or suggest wherein a frequency of the driving waveform is based on a linearly translated input source voltage". Gray apparently discloses, in Fig. 2A and paragraph [0060], lines 1-9, that the frequency of the driving waveform would increase as the battery voltage increases, and that the frequency cannot change when the VCO [220] achieves its maximum frequency, irrespectively of further increases in the battery voltage. As such, Gray truly teaches that the frequency of the driving waveform is based on the linearly translated input source voltage as claimed. Therefore, claims 1-4 remain rejected as being anticipated by Gray (see Claims Rejections under 35 U.S.C. § 102 set forth in this Office Action for details).

With respect to the limitation "wherein the frequency is based on a range of input source voltages and a range of desired linearly translated source voltages associated with the PZT" recited in amended claims 5 and 6 and referred to respectively in the second and third paragraphs at page 6 of the amendment, Applicant is suggested to direct attention to the circuitry of Fig. 2A and the description provided in paragraphs [0050, 0060]. Gray clearly discloses that the

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frequency of the driving waveform is based on a range of input source voltages (which is VR1 ranging from 0.5 to 3 Volts; see paragraph [0050], lines 5-6) and a range of desired linearly translated source voltages associated with the PZT (which is provided by battery source [101]; see paragraph [0060], lines 1-9). Therefore, claims 5-7 remain rejected as being anticipated by Gray (see Claims Rejections under 35 U.S.C. § 102 set forth in this Office Action for details).

With respect to Applicant's argument on claim 8 in the fifth paragraph at page 6 of the amendment, the Examiner agrees that the signal OUTAPB is not a "high voltage source" in a common sense but it is "high" with respect to other sources in the circuit. As clearly addressed above, Gray discloses an arrangement including a first resistor [216] coupled between a node [N6] and a high voltage source (which is VOH, high level of signal OUTAPB; see paragraph [0056], lines 2-3), wherein the high voltage source is one voltage in the range of input source voltages (e.g. VR1). Therefore, claims 8-9 remain rejected as being anticipated by Gray (see Claims Rejections under 35 U.S.C. § 102 set forth in this Office Action for details).

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

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however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuy V. Tran whose telephone number is (571) 272-1828. The examiner can normally be reached on M-F (8:00 AM -5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Wong can be reached on (571) 272-1834. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thuy V. Tran
Primary Examiner
Art Unit 2821

10/17/2004